Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF THE CLAIMS:

1. (Currently Amended) A multi-node network of processors, comprising:

a network;

a plurality of processors coupled in said network, said processors having a minimally operational state, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request; and having a fully operational state employing a code image[,]; said processors, when in said minimally operational state, requesting said code image from said network; and

a master source coupled in said network, said master source having at least said code image for broadcasting said code image on said network, said master source, upon receiving said code image request, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state, and, upon completion of said predetermined time period, broadcasting said code image on said network.

2. (Original) The multi-node network of processors of Claim 1, wherein said processors, additionally, upon said broadcast of said code image, receive and implement said code image only if said processor is in said minimally operational state.

3. (Original) The multi-node network of processors of Claim 1, wherein said processors additionally each comprises a non-volatile memory for storing said minimally operational state code.

4. (Original) The multi-node network of processors of Claim 3, wherein said minimally operational state code comprises a boot program which becomes operational upon reboot of said processor.

5. (Original) The multi-node network of processors of Claim 3, wherein said code for said minimally operational state is additionally sufficient to conduct at least a basic system test and provide said code image request.

6. (Original) The multi-node network of processors of Claim 1, wherein said processors additionally comprise a RAM for, upon receiving said code image, storing said code image.

7. (Original) The multi-node network of processors of Claim 1, wherein said master source provides one said code image for any said code image request.

8. (Original) The multi-node network of processors of Claim 7, wherein ones of said processors implement different said code images, wherein said one master source code image comprises a combination of said different code images, and wherein said processors additionally select and implement one of said combination of different code images.

9. (Original) The multi-node network of processors of Claim 1, wherein said master source comprises a plurality of different said code images, wherein said processor requesting said code image requests one of said different code images, wherein said master source broadcasts said requested one of said different code images, and wherein said processors additionally determine whether said broadcast code image is correct for said processor, and select said broadcast code image for implementation if said determination determines that said code image is correct for said processor.

10. (Currently Amended) A method for providing a code image for processing nodes of a multi-node network of processors, comprising the steps of:

at least one said processor, comprising a node of said network, in a minimally operational state, requesting said code image from said network; said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request;

a master source, upon receiving said code image request, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state; and

said master source, upon completion of said predetermined time period, broadcasting said code image on said network.

11. (Original) The method of Claim 10, additionally comprising the step of, said processors, upon said broadcast of said code image, receiving and implementing said code image only if said processor is in said minimally operational state.

12. (Original) The method of Claim 10, wherein said code of said minimally operational state is stored in a non-volatile memory.

13. (Original) The method of Claim **12**, wherein said minimally operational state additionally comprises operation of a boot program which becomes operational upon reboot of said processor.

14. (Original) The method of Claim **12**, wherein said minimally operational state of said processor comprises having said non-volatile code additionally sufficient to conduct at least a basic system test and provide said code image request.

15. (Original) The method of Claim **10**, additionally comprising the step of, said processor, upon receiving said code image, storing said code image in RAM.

16. (Original) The method of Claim **10**, wherein one said code image is provided by said master source for any said code image request.

17. (Original) The method of Claim **16**, wherein ones of said processors implement different said code images, wherein said one code image provided by said master source comprises a combination of said different code images, and wherein said method additionally comprises the step of, said processors selecting and implementing one of said combination of different code images.

18. (Original) The method of Claim **10**, wherein said master source comprises a plurality of different said code images, wherein said step of said processor requesting said code image comprises requesting one of said different code images, wherein said step of said master source broadcasting said code image comprises broadcasting said requested one of said different code images, and wherein said method additionally comprises the step of, a receiving said processor determining whether said broadcast code image is correct for said processor, and selecting said code image for implementation if said determination step determines that said code image is correct for said processor.

19. (Currently Amended) For a multi-node network of processors, said network having a plurality of processors coupled in said network, said processors having a minimally operational state, and having a fully operational state employing a code image, said processors, when in said minimally operational state, requesting said code image from said network, a master source comprising:

a master interface coupled in said network;

a memory storing at least said code image for said processors of said network; and

a master processor coupled to said memory and to said master interface, upon receiving said code image request at said master interface, waiting a predetermined time period, said predetermined time period allowing any additional said processor

to reach [said] a minimally operational state, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request; and, upon completion of said predetermined time period, broadcasting said code image stored in said memory, via said master interface, on said network.

20. (Original) The master source for said multi-node network of processors of Claim **19**, wherein said master processor provides one said code image for any said code image request.

21. (Original) The master source for said multi-node network of processors of Claim **20**, wherein ones of said processors implement different said code images, and wherein said one master source code image stored in said memory and broadcast by said master processor comprises a combination of said different code images, such that said processors additionally select and implement one of said combination of different code images.

22. (Original) The master source of said multi-node network of processors of Claim **19**, comprising a plurality of different said code images, wherein said processor requesting said code image requests one of said different code images, wherein said master source master processor selects from said memory and broadcasts said requested one of said different code images, such that a

receiving said processor additionally determines whether said broadcast code image is correct for said processor, and selects said broadcast code image for implementation if said determination determines that said code image is correct for said processor.

23. (Currently Amended) For a multi-node network of processors, said network having a master source coupled in said network, said master source having a code image for broadcasting on said network, said master source, upon receiving ~~said~~ a code image request, waiting a predetermined time period, said predetermined time period allowing any additional processor to reach ~~said~~ a minimally operational state, and, upon completion of said predetermined time period, broadcasting said requested code image on said network, a processor comprising:

a processor interface coupling said processor in said network;

a non-volatile memory for storing code providing a minimally operational state of said processor, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request;

a processor memory capable of storing a code image providing a fully operational state of said processor; and

a processing unit coupled to said non-volatile memory, said processor memory and said processor interface, when in said minimally operational state provided by said non-volatile memory, requesting said code image from said network, via said processor interface.

24. (Original) The processor for a multi-node network of processors of Claim **23**, wherein said processing unit, additionally, upon said broadcast of said code image by said master source, receives and stores said code image in said processor memory, and implements said code image, only if said processing unit is in said minimally operational state.

25. (Original) The processor for a multi-node network of processors of Claim **23**, wherein said minimally operational state code stored in said non-volatile memory comprises a boot program which is provided to said processing unit and becomes operational upon reboot of said processor.

26. (Original) The processor for a multi-node network of processors of Claim **25**, wherein said boot program stored in said non-volatile memory storing for said minimally operational state is additionally sufficient to conduct at least a basic system test and provide said code image request.

27. (Original) The processor for a multi-node network of processors of Claim **23**, wherein said processor memory comprises a RAM for storing said code image.

28. (Original) The processor for a multi-node network of processors of Claim **23**, wherein said master source provides one said code image for any said code image request, said one code image comprising a combination of said different code images, and wherein ones of said processors implement different said one code images, said processing unit additionally selecting, storing and implementing one of said combination of different code images.

29. (Original) The processor of a multi-node network of processors of Claim **23**, wherein said master source comprises a plurality of different said code images, said master source broadcasting said requested one of said different code images, and wherein said processor requesting said code image requests one of said different code images, said processor additionally determines whether said broadcast code image is correct for said processor, and selects said broadcast code image for implementation if said determination determines that said code image is correct for said processor.

30. (Currently Amended) A computer program product usable with a programmable computer having computer readable program code embodied therein, said programmable computer comprising a master source coupled in a network, said network having a plurality of processors coupled in said network, said processors having a minimally operational state, and having a fully operational state employing a code image, said processors, when in said minimally operational state, requesting said code image from said network, said computer program product comprising:

computer readable program code which causes said master source programmable computer to store at least said code image;

computer readable program code which causes said master source programmable computer to, upon receiving ~~said~~ a code image request, wait a predetermined time period, said predetermined time period allowing any additional said processor to reach ~~said~~ a minimally operational state, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request; and

computer readable program code which causes said master source programmable computer to, upon completion of said time period, broadcast said stored code image on said network.

31. (Original) The computer program product of Claim **30**, wherein ones of said processors implement different said code images; wherein said stored code image comprises a combination of said different code images; and wherein said computer readable program code which causes said master source computer processor to broadcast said stored code image, causes said master source computer processor to broadcast said code image combination of said different code images as one code image, such that said processors additionally select and implement one of said combination of different code images.

32. (Original) The computer program product of Claim **30**, wherein said stored code image comprises a plurality of different said code images, wherein said processor requesting said code image requests one of said different code images, and wherein said computer readable program code which causes said master source computer processor to broadcast said stored code image, causes said master source computer processor to broadcast said requested one of said different code images, such that said processors additionally determine whether said broadcast code image is correct for said processor, and select said broadcast code image for implementation if said determination determines that said code image is correct for said processor.

33. (Currently Amended) A method for updating code images for processors of modules of a redundant system, said redundant system comprising at least two sets of redundant said modules, said processors comprising nodes of a multi-node network of processors, said processors having a minimally operational state and requiring a code image to become fully operational, said processors, when in said minimally operational state, request said code image from said network, said method comprising the steps of:

providing a reboot of at least one said set of redundant modules, such that said processors of said modules reach ~~said~~ a minimally operational state and request said code image from said network, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request;

a master source, upon receiving said code image request, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state;

said master source, upon completion of said predetermined time period, broadcasting said code image on said network, such that said processors requesting said code image become fully operational;

providing a reboot of a remaining at least one said set of redundant modules, such that said processors of said modules

reach said minimally operational state and request said code image from said network;

said master source, upon receiving said code image request, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state; and

said master source, upon completion of said predetermined time period, broadcasting said code image on said network, such that said processors of said remaining set of redundant modules requesting said code image become fully operational.

34. (Currently Amended) A computer program product usable with a programmable computer having computer readable program code embodied therein, said programmable computer comprising a master source coupled in a network, for updating code images for processors of modules of a redundant system, said redundant system comprising at least two sets of redundant said modules, said processors comprising nodes of a multi-node network of processors, said processors having a minimally operational state and requiring a code image to become fully operational, said processors, when in said minimally operational state, request said code image from said network said computer program product comprising:

computer readable program code which causes said master source programmable computer to store at least an update of said code image;

computer readable program code which causes said master source programmable computer to provide a reboot of at least one said set of redundant modules, such that said processors of said modules reach ~~said~~ a minimally operational state, said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request; and request said code image from said network;

computer readable program code which causes said master source programmable computer to, upon receiving said code image request, wait a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state;

computer readable program code which causes said master source programmable computer to, upon completion of said predetermined time period, broadcast said code image on said network, such that said processors requesting said code image become fully operational;

computer readable program code which causes said master source programmable computer to provide a reboot of a remaining at least one said set of redundant modules, such that said processors of said modules reach said minimally operational state and request said code image from said network;

computer readable program code which causes said master source programmable computer to, upon receiving said code image request, wait a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state; and

computer readable program code which causes said master source programmable computer to, upon completion of said predetermined time period, broadcast said code image on said network, such that said processors of said remaining set of redundant modules requesting said code image become fully operational.

35. (Currently Amended) A multi-node network of processors, comprising:

a network;

a first set of redundant processors coupled in said network, said processors having a minimally operational state, <u>said minimally operational state absent a code image required to become fully operational, said minimally operational state sufficient to provide a code image request;</u> and having a fully operational state employing a code image[,]<u>;</u> said processors, when in said minimally operational state, requesting said code image from said network;

a second set of redundant processors coupled in said network, said processors having a minimally operational state,

and having a fully operational state employing a code image, said processors, when in said minimally operational state, requesting said code image from said network; and

a master source coupled in said network, said master source having at least said code image for broadcasting said code image on said network, said first set of redundant processors rebooted to said minimally operational state, said master source, upon receiving said code image request from one of said first set of redundant processors, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state, and, upon completion of said predetermined time period, broadcasting said code image on said network, whereby said first set of redundant processors become fully operational; whereupon said second set of redundant processors are subsequently rebooted to said minimally operational state, said master source, upon receiving said code image request from one of said second set of redundant processors, waiting a predetermined time period, said predetermined time period allowing any additional said processor to reach said minimally operational state, and, upon completion of said predetermined time period, broadcasting said code image on said network, whereby said second set of redundant processors become fully operational.